FIG. 1

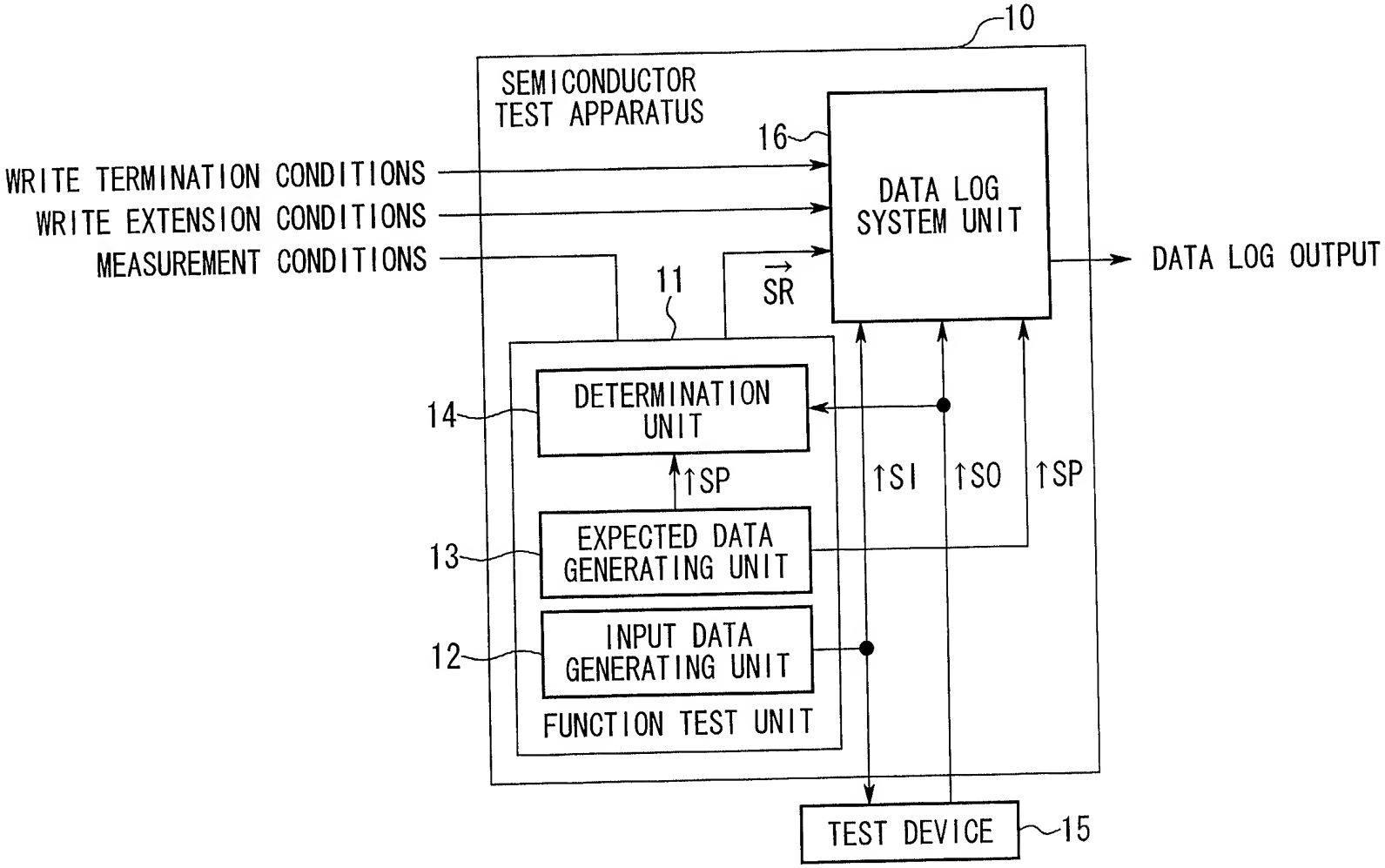

10
SEMICONDUCTOR TEST APPARATUS
16
DATA LOG SYSTEM UNIT
WRITE TERMINATION CONDITIONS
WRITE EXTENSION CONDITIONS
MEASUREMENT CONDITIONS
DATA LOG OUTPUT
11
SR
14
DETERMINATION UNIT
↑SP
↑SI
↑SO
↑SP
13
EXPECTED DATA GENERATING UNIT
12
INPUT DATA GENERATING UNIT
FUNCTION TEST UNIT
TEST DEVICE
15

FIG. 2

LOG MEMORY ADDRESS	MEASUREMENT INPUT DATA	MEASUREMENT RESULT DATA	MEASUREMENT EXPECTATION DATA	MEASUREMENT DETERMINATION DATA
0	0	HIGH	HIGH	PASS
1	1	LOW	LOW	PASS
2	2	HIGH	HIGH	PASS
3	3	LOW	LOW	PASS
4	0	HIGH	HIGH	PASS
5	1	LOW	LOW	PASS
6	2	HIGH	HIGH	PASS
7	3	HIGH	LOW	FAIL
~	~	~	~	~
n-1	62	HIGH	HIGH	PASS
n	63	LOW	LOW	PASS

FIG. 3

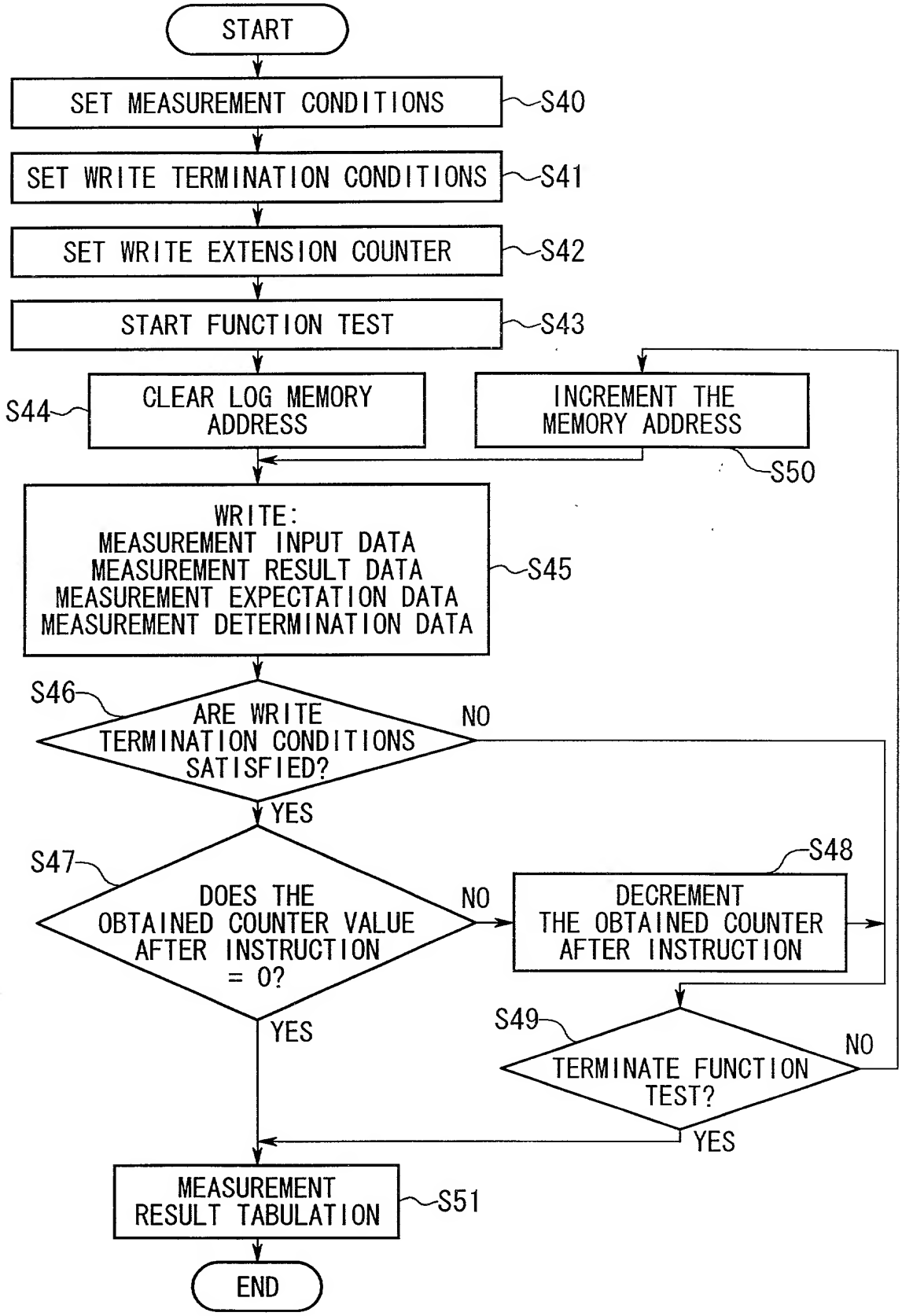

START
SET MEASUREMENT CONDITIONS
S40
SET WRITE TERMINATION CONDITIONS
S41
SET WRITE EXTENSION COUNTER
S42
START FUNCTION TEST
S43
S44
CLEAR LOG MEMORY ADDRESS
INCREMENT THE MEMORY ADDRESS
S50
WRITE:
MEASUREMENT INPUT DATA
MEASUREMENT RESULT DATA
MEASUREMENT EXPECTATION DATA
MEASUREMENT DETERMINATION DATA
S45
S46
ARE WRITE TERMINATION CONDITIONS SATISFIED?
NO
YES
S47
DOES THE OBTAINED COUNTER VALUE AFTER INSTRUCTION = 0?
NO
S48
DECREMENT THE OBTAINED COUNTER AFTER INSTRUCTION
YES
S49
TERMINATE FUNCTION TEST?
NO
YES
MEASUREMENT RESULT TABULATION
S51
END

FIG. 4

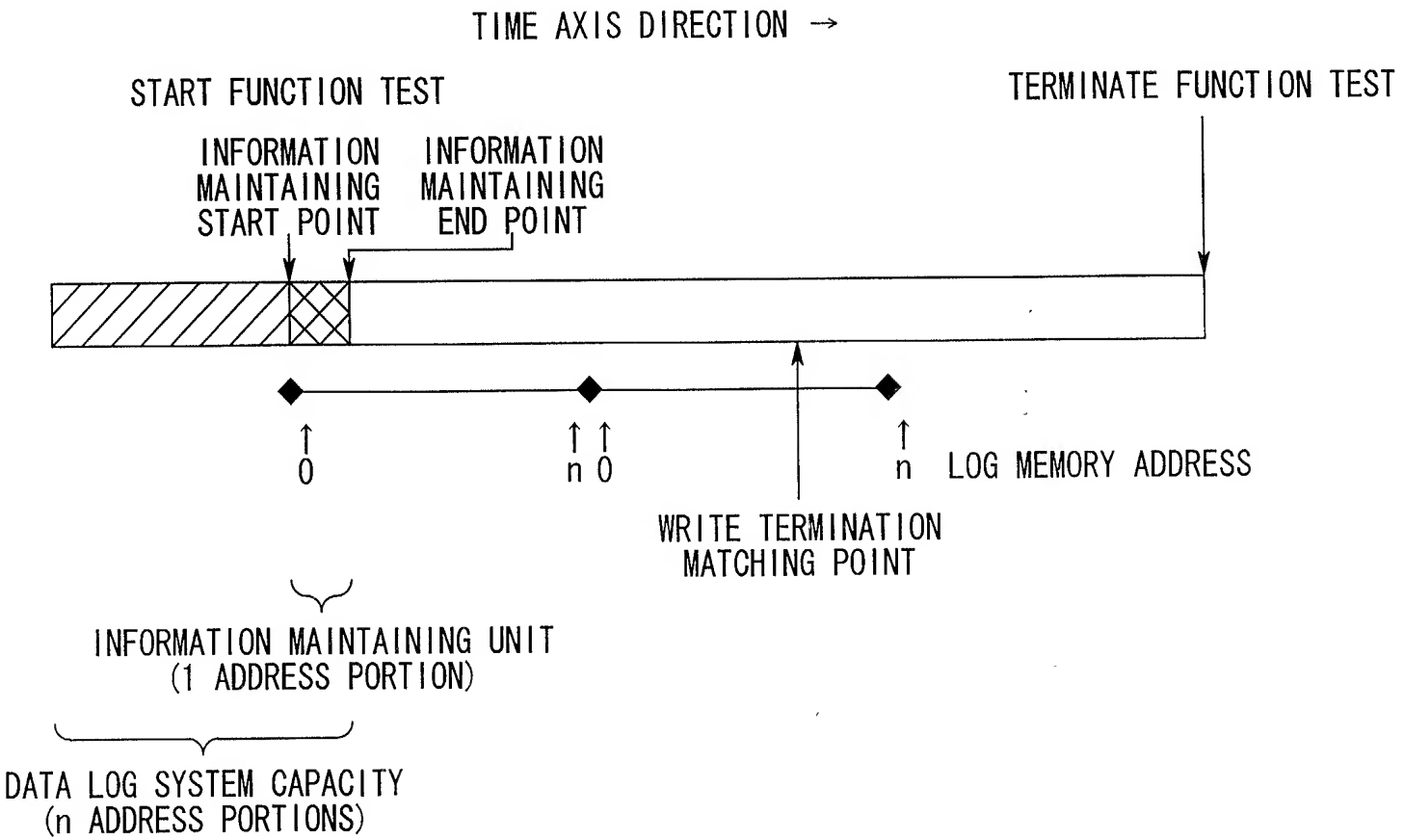

TIME AXIS DIRECTION →
START FUNCTION TEST
TERMINATE FUNCTION TEST
INFORMATION MAINTAINING START POINT
INFORMATION MAINTAINING END POINT
0
n 0
n
LOG MEMORY ADDRESS
WRITE TERMINATION MATCHING POINT
INFORMATION MAINTAINING UNIT (1 ADDRESS PORTION)
DATA LOG SYSTEM CAPACITY (n ADDRESS PORTIONS)

FIG. 5

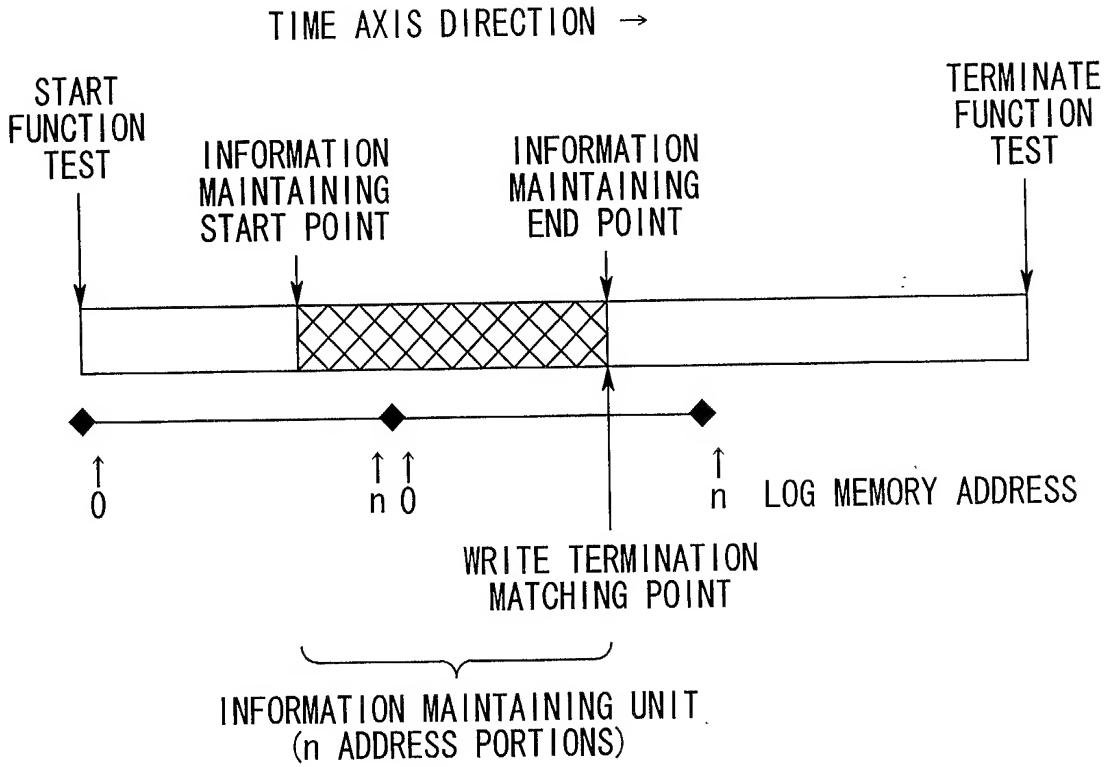

TIME AXIS DIRECTION →
START FUNCTION TEST
INFORMATION MAINTAINING START POINT
INFORMATION MAINTAINING END POINT
TERMINATE FUNCTION TEST
0
n 0
n
LOG MEMORY ADDRESS
WRITE TERMINATION MATCHING POINT
INFORMATION MAINTAINING UNIT (n ADDRESS PORTIONS)

FIG. 6

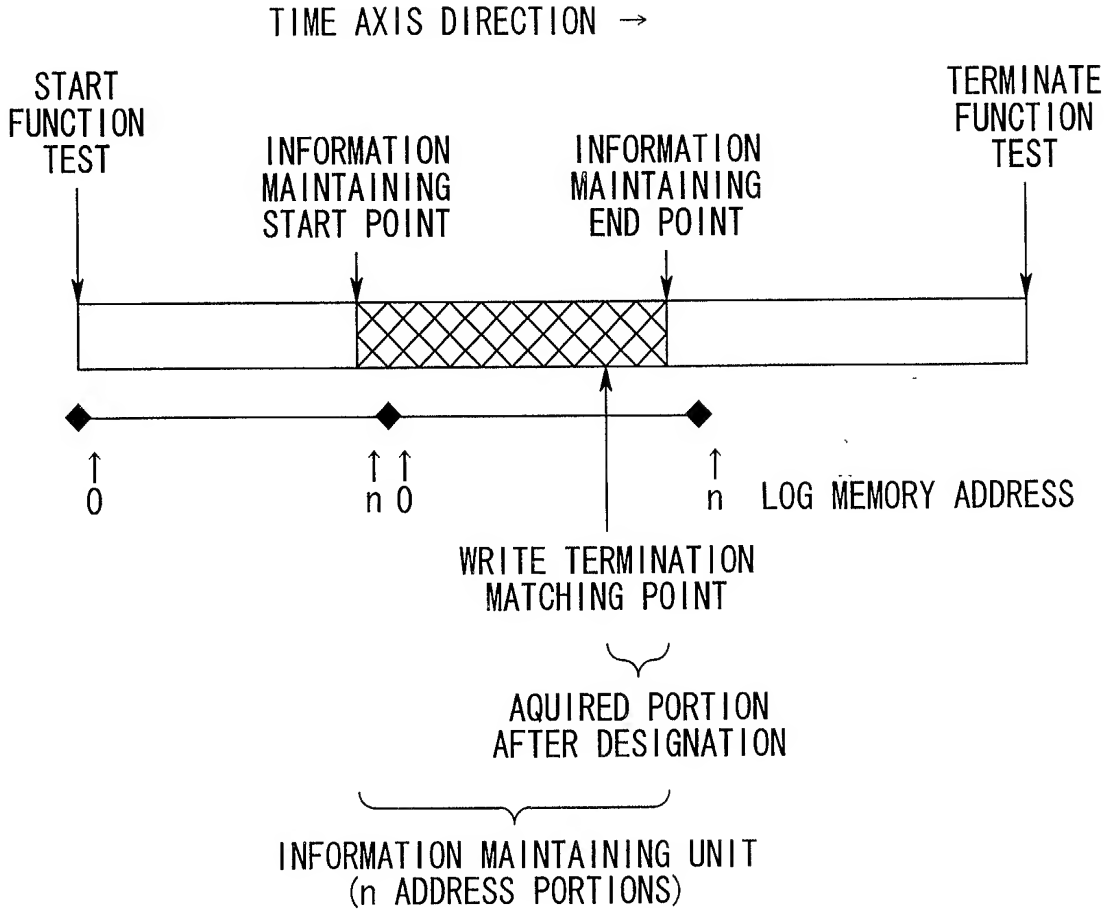

TIME AXIS DIRECTION →
START FUNCTION TEST
INFORMATION MAINTAINING START POINT
INFORMATION MAINTAINING END POINT
TERMINATE FUNCTION TEST
0
n 0
n
LOG MEMORY ADDRESS
WRITE TERMINATION MATCHING POINT
AQUIRED PORTION AFTER DESIGNATION
INFORMATION MAINTAINING UNIT
(n ADDRESS PORTIONS)

FIG. 7

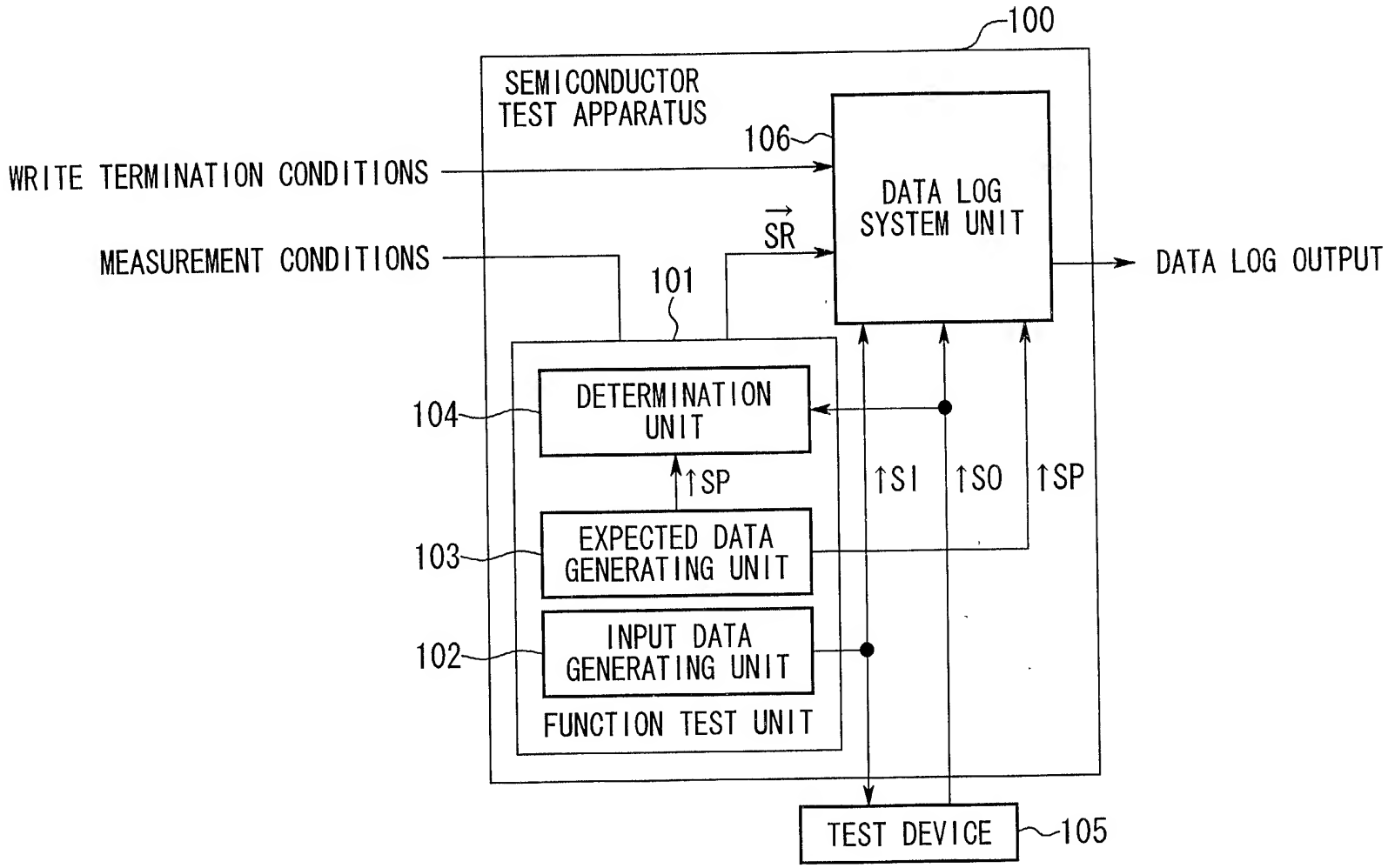
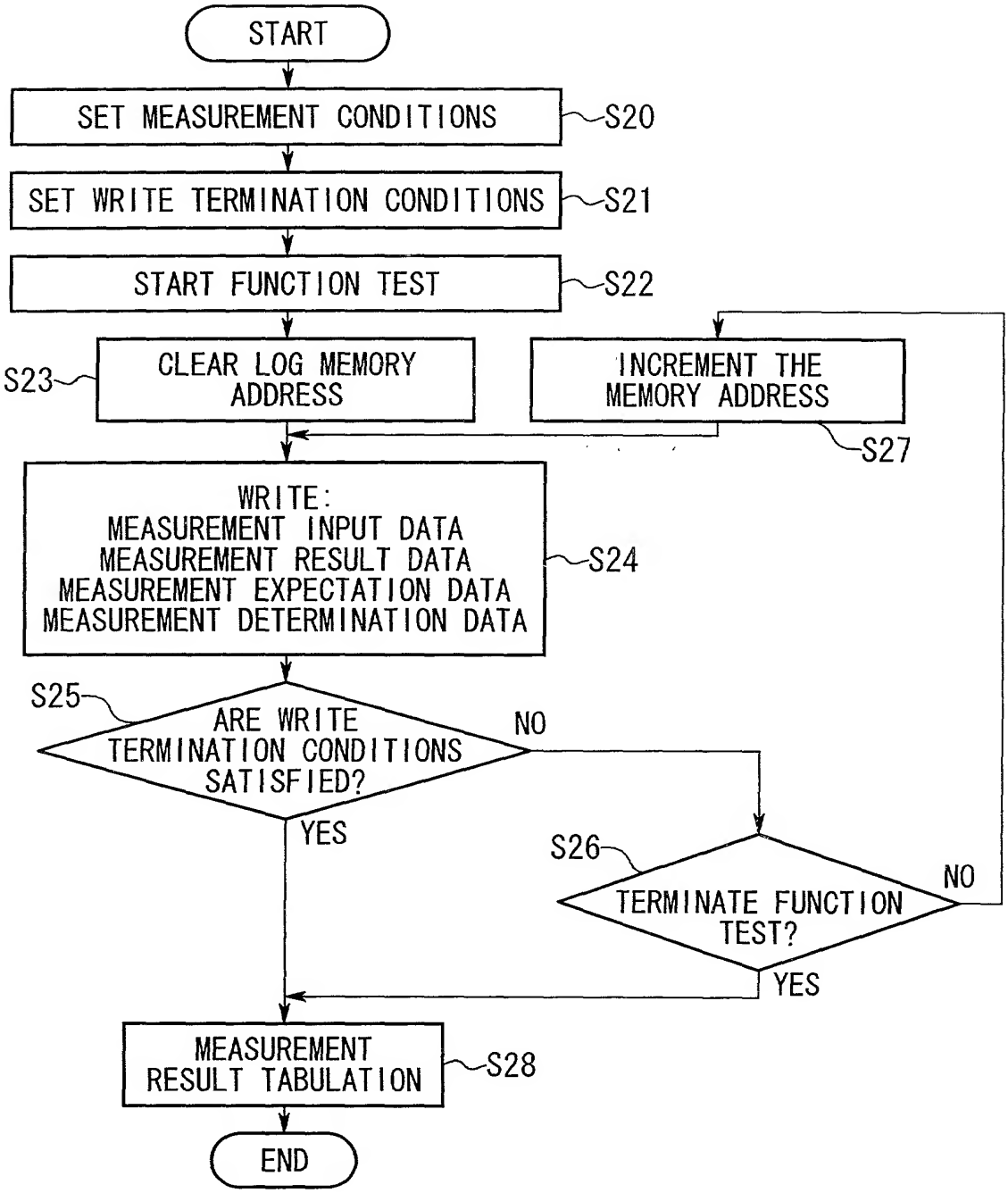

100
SEMICONDUCTOR TEST APPARATUS
106
WRITE TERMINATION CONDITIONS
MEASUREMENT CONDITIONS
DATA LOG SYSTEM UNIT
SR
DATA LOG OUTPUT
101
104
DETERMINATION UNIT
↑SP
↑SI
↑SO
↑SP
103
EXPECTED DATA GENERATING UNIT
102
INPUT DATA GENERATING UNIT
FUNCTION TEST UNIT
TEST DEVICE
105

FIG. 8


START
SET MEASUREMENT CONDITIONS
S20
SET WRITE TERMINATION CONDITIONS
S21
START FUNCTION TEST
S22
S23
CLEAR LOG MEMORY ADDRESS
INCREMENT THE MEMORY ADDRESS
S27
WRITE:
MEASUREMENT INPUT DATA
MEASUREMENT RESULT DATA
MEASUREMENT EXPECTATION DATA
MEASUREMENT DETERMINATION DATA
S24
S25
ARE WRITE TERMINATION CONDITIONS SATISFIED?
NO
YES
S26
TERMINATE FUNCTION TEST?
NO
YES
MEASUREMENT RESULT TABULATION
S28
END